CLAIMS

1. Method of manufacturing an edge structure for a high voltage semiconductor device, comprising a first step of forming a first semiconductor layer of a first conductivity type, a second step of forming a first mask over the top surface of said first semiconductor layer, a third step of removing portions of said first mask in order to form at least one opening in it, a fourth step of introducing dopant of a second conductivity type in said first semiconductor layer through said at least one opening, a fifth step of completely removing said first mask and of forming a second semiconductor layer of the first conductivity type over said first semiconductor layer, a sixth step of diffusing the dopant implanted in said first semiconductor layer in order to form a doped region of the second conductivity type in said first and second semiconductor layers, repeating at least one time the second step up to the sixth step in order to form a final edge structure comprising a number of superimposed semiconductor layers of the first conductivity type and at least two columns of doped regions of the second conductivity type, said columns being inserted in said number of superimposed semiconductor layers and formed by superimposition of said doped regions subsequently implanted through the mask openings, the column near said high voltage semiconductor device being deeper than the column farther from said high voltage semiconductor device.

2. Manufacturing method according to claim 1, wherein said superimposed doped regions of each column are vertically merged to each other.

3. Manufacturing method according to claim 1, wherein said superimposed doped regions of each column are not vertically merged to each other.

4. Manufacturing method according to claim 1, wherein each mask for forming said column of doped regions has an additional opening in respect to the preceding mask, said additional opening being properly distanced from the preceding opening in order to form an additional column.

5. Manufacturing method according to claim 1, wherein said mask is a photoresist layer.

6. Manufacturing method according to claim 1, comprising the step of forming an oxide layer over the top surface of each one of said semiconductor layers before the formation of said mask, and the removal of said oxide layer during the removal of said mask.

7. Manufacturing method according to claim 6, wherein said oxide layer has a thin thickness suitable to not prevent the subsequent steps of introducing dopant.

8. Manufacturing method according to claim 1, wherein said step of introducing dopant is a ion implantation.

9. Manufacturing method according to claim 1, wherein said high voltage semiconductor device is a power MOSFET.

10. Manufacturing method according to claim 1, wherein said first semiconductor layer is epitaxially grown over a semiconductor substrate of the first conductivity type.

11. Manufacturing method according to claim 1, wherein said first type of conductivity is the N type and said second type of conductivity is the P type.

12. Manufacturing method according to claim 1, wherein said first type of conductivity is the P type and said second type of conductivity is the N type.

13. An integrated edge structure for a high voltage semiconductor device, comprising a number of superimposed semiconductor layers of a first conductivity type and at least two columns of doped regions of a second conductivity type, said columns being inserted in said number of superimposed semiconductor layers, the column near said high voltage semiconductor device being deeper than the column farther from said high voltage semiconductor device.

14. The integrated edge structure according to claim 13, wherein said high voltage

semiconductor device is a power MOSFET.

15. The integrated edge structure according to claim 13, wherein said number of superimposed semiconductor layers is superimposed to a semiconductor substrate.

16. The integrated edge structure according to claim 13, wherein each one of said at least two columns has a depth decreasing by shifting from said high voltage semiconductor device towards the outside.

17. The integrated edge structure according to claim 13, wherein the doped regions of each one of said at least two columns are superimposed and vertically merged to each other.

18. The integrated edge structure according to claim 13, wherein the doped regions of each of said at least two columns are superimposed but not merged to each other.

19. The integrated edge structure according to claim 13, wherein said first type of conductivity is the N type and said second type of conductivity is the P type.

20. The integrated edge structure according to claim 13, wherein said first type of conductivity is the P type and said second type of conductivity is the N type.